REMARKS

Pending Claims:

In this application, claims 1, 4, 5, 7-14, 16-18, and 23-37 are currently pending. Claims 1, 6, 8, 9, 11, 13, 16-18, 23-27, 29, 32 33, and 35 are amended by this Response. Claims 12 remains unchanged since filing. Claims 4, 5, 8, 10, 14, 28, 31, 32, and 34 were previously presented. Claims 2, 3, 6, 15, and 19-22 have been deleted. Claims 36 and 37 have been added. Entry of these amendments is respectfully requested.

Rejection under 35 U.S.C. §112

Claim 1 was rejected because of a limitation referring to a "deferred header queue" for which there was no antecedent basis. The relevant clause of claim 1 now states, "a deferred header queue containing entries having destination and buffer address information for data to be deferred, with entries for data addressed to multiple destinations ports being intermingled within the deferred header queue." This fixes the antecedent basis problem.

Rejection under 35 U.S.C. §103

Claim 1 was also rejected for obviousness over Yamada (US 5,455,820) in view of Yamanaka (US 5,619,495) and Merchant et al. (US 6,904,043. This rejection was addressed in an interview between Applicant represented by myself, its attorney and Examiner Mered on August 15, 2006. In preparation for that interview, Applicant responded to the obviousness rejection in a letter dated August 14, 2006. That argument is presented below, and is followed by a summary of the interview.

Regarding the "intermingling" limitation of claim 1, in par. 7 on p.3 the Office Action states, "Yamada teaches a deferred queue having entries having destination and buffer address information for data to be deferred, with entries for data addressed to multiple destination ports being intermingled within the deferred queue. (See Column 5, Lines 1-15)"

Both Yamada and the present invention deal with the head of line blocking problem, but in distinct ways. In particular, they are very different with respect to handling the situation when two or more destination locations are congested. Yamada has a plurality of cell buffers (col. 3 ll. 47-51). When none of the destinations is congested, one of the buffers receives all the cells and sends them on their destinations

(col. 4 ll. 3-11); furthermore, "the other cell buffers will be used when overflow occurs in any of the output buffer sections."

Fig. 4(a) shows how the input cell buffer is identified when an overflow occurs. If the first spare buffer is "idle," all cells addressed to the congested destination get sent to the first spare cell buffer (S11, S12, S14, S17). If overflow occurs at a second destination, then cells headed for the second congested destination will go to the second spare cell buffer (S11, S12, S13, S15). Moreover, if the number of simultaneously congested destinations exceeds the number of spare buffers, S17 says to "command address filter to check cells addressed to overflown output buffer section and to prevent those cells from gating." In other words, the cells are discarded and never transmitted. The text cited in the Office Action (i.e., col. 5 ll. 1-15) is consistent with Fig. 4(a) and does not indicate intermingling of data intended for distinct congested destinations.

Once a destination is no longer congested, Fig. 4(b) step S24 causes "all cells" to be "fed out from spare cell buffer." This is consistent with the description, which again states that "all the cells are output from the spare cell buffer." (Col. 5 ll. 15-32). If all cells are emptied from the spare cell buffer when just one destination of several congested ones recovers, it must mean that the spare cell buffer only contains data targeted for a single destination.

In short, Yamada does not intermingle "entries for data addressed to multiple destination ports." This is a significant disadvantage—as has already been noted, if there are too few buffers to handle all congested destinations, data are simply thrown away. So why not just have one buffer for each destination? That is, of course, possible, but is a huge waste of buffer storage space.

Yamanaka is cited for teaching "a cell switching system having buffer memories in which accesses of a plurality of cells can be implemented in one cell time." Thus, Yamanaka is irrelevant to the intermingling limitation.

Yamada does not store and examine headers (containing destination address) independently from the associated data content (e.g., frame). The principal and spare buffers hold whole cells, both destination address and content. Merchant has been cited as standing for separate storage and examination of headers. Merchant, however, deals with congestion on a serial line coming into a switch input. It does not deal with congestion at the switch output destinations. Merchant does not defer headers at all; rather, it places them into queues, one queue for each switch input port. (Fig. 4)

Under the assumption that Merchant stands for the concept of separating headers from data content, and if Merchant is combined with Yamada, the result is a set of buffers that contain headers rather than data cells. When a destination is congested, its headers would be rerouted to a single spare buffer allocated to the congested destination until it manages to clear itself. When the congestion clears for a given destination, the spare buffer for that destination would be drained of "all" the headers it contains. The remarks above related to wasted storage and data being lost in Yamada's scheme still pertain if headers are stored and examined separately from cells.

In the present invention as stated in claim 1, entries in the deferred header queue are intermingled. If, say, 100 destination ports are simultaneously congested, there is no need for 100 separate buffers as in Yamada—only 1 is needed. Actually, there are two kinds of intermingling in the present invention: deferred headers are intermingled in the deferred header queue [0006 in the published application, namely, US 2003/0112818 A1], and deferred frames are intermingled in a buffer memory [0005]. Each of the independent claims that were submitted previously in the response mailed February 10, 2006 to the previous Office Action contained some aspect of intermingling data for two or more congested destinations. For example, claim 10 includes "a deferred header queue for storing frame information for packets/frames being deferred, the deferred header queue device containing packets/frames addressed to more than one destination port.

Interview Regarding Obviousness Rejection

The obviousness rejections of the independent claims were discussed in a phone interview held on August 15, 2006. An interview summary prepared by Examiner Mered and mailed on August 23, 2006 states that:

- Claims 1, 10, 18, 26, and 35 were discussed;
- The patent to Yamada (U.S. 5,455,820) was discussed;
- Agreement on the claims was reached. and Applicant convincingly argued that Yamada (US 5,455,820) fails to address the limitation in claim 1 specifying entries in the deferred header are intermingled in one queue/buffer while Yamada assigns a specific spare buffer for cells destined to a specific an unavailable output buffer and consequently no intermingling occurs. Examiner concurred with Applicant that Yamada fails to teach this

specific limitation. Further Applicant agreed that in all the independent claims 1, 10, 18, 26, and 35 deferred queue has to be replaced by deferred header queue and what is contained in the deferred header queues has to be corrected and clarified in all the independent claims.

Claim Elements in the Newly Amended Claims Distinguishing Prior Art

The existing claims were modified consistently with the conclusions of the interview. All claims now involve intermingling in a deferred header queue of destination entries for deferred data. All changes to the existing claims, as well as the two new claims, are supported by the description and drawings.

Independent claim 1 was amended, as discussed above, to remedy the antecedent basis problem. It now states that the deferred header queue contains "entries for data addressed to multiple destination ports being intermingled within the deferred header queue," and hence clearly contains destination intermingling making it distinguishable over the prior art. Claims 8 and 9, both ultimately dependent upon claim 1, were amended to clarify their grammar. Independent claim 1, and claims 4, 5, and 7-9, which depend ultimately on claim 1, should now all be in condition for allowance.

Independent claim 10 formerly included the element of "a deferred header queue device for storing frame information for packets/frames being deferred, the deferred header queue device containing packets/frames addressed to more than one destination port." This language has been modified as proposed in Applicant's letter to Examiner Mered in preparation for the interview to contain the phrase "information for" prior to the word "containing." This language clarifies that the deferred header queue contains information about the packets/frames, not the packets/frames themselves. The prior art is distinguished because the information is "for packets/frames addressed to more than one destination port." Dependent claim 16 is more specific, stating that "the stored frame information comprises header information and a starting address in the buffer memory for the packet/frame." Other changes to claims depending ultimately on claim 10 include the following:

- A grammatical correction was made to claim 11;
- In claim 13, the term "header queue" was changed to "header queue device" for consistency with base claim 10;

- The preamble of claim 16 has been changed from referring to "The buffer control apparatus" to "The deferred queue device," for consistency with claim 10 to which it refers; the preamble of claim 17 has been changed correspondingly to be consistent with that of its base claim 12.

Independent claim 10 and claims 11-14, 16, and 17, which ultimately depend on claim 10, should now all be in condition for allowance.

Independent claim 18 (i.e., 18.a.iii) formerly included the step of "deferring transmission of the data ... by storing the *data* to be deferred in a *deferred queue* whereby data addressed to different destination ports are simultaneously stored in the same deferred queue." (Emphasis added.) In other words, the data are intermingled in a deferred queue. This language has been changed to "deferring transmission of the data ... by storing *entries including destinations* for the data to be deferred in a *deferred header queue* simultaneously containing entries corresponding to data addressed to different destination ports." Claim 18 as now amended clearly deals with entries stored in a deferred header queue that contain destination information regarding the deferred data. It also contains the intermingling concept as a limitation. Claim 23, which depends on claim 18, has been amended analogously to describe a "backup header queue" (rather than a backup queue) in which "entries including destinations for data received during the deferred state" are stored. Claims 24 and 25 were amended consistently as well. Therefore independent claim 18 and claims 23-25, which ultimately depend on claim 18, should be allowed.

Independent claim 26 and associated dependent claims have been modified similarly. Of particular relevance is limitation 26.c, which now clearly refers to a "deferred header queue in which destination entries for data for a plurality of different output ports having a negative transmission status are tracked." This limitation contains the concept of intermingling of entries containing destination information in a deferred header queue. Claims 27, 29 32, and 33, all dependent ultimately on claim 26, have been amended consistently. Independent claim 26, as well as dependent claims 27-35, should all now be allowed.

New Claims:

Claims 36 and 37 are new. These claims are also patentable over the prior art because they capture the concept of destination information corresponding to deferred data for two output ports in a buffered switch that are intermingled in a deferred header queue.

CONCLUSION

All of the claims remaining in this application should now be seen to be in condition for allowance. The prompt issuance of a notice to that effect is solicited.

Respectfully submitted,
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